CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1-15. **(Cancelled)**

16. **(Currently Amended)** An information handling system comprising:

a processor;

a memory communicatively coupled to the processor;

and a circuit board **communicatively coupled to the processor, the circuit board ~~having an electrical trace, the circuit board operable to reduce noise on the electrical trace induced from a reference plane, the circuit board including~~ comprising**:

a voltage plane forming a first layer of the circuit board, the voltage plane operable to provide an electrical current;

a ground plane forming a second layer of the circuit board, the ground plane operable to provide a ground for the electrical current;

[[an]] **the** electrical trace routed over a portion of the circuit board, the electrical trace including a first path and a second path such that the first path references the ground plane and the second path references the voltage plane whereby the first path is substantially similar to the second path; and

the first path electrically coupled to the second path at each of the ends of the paths. **~~such that noise induced into the electrical trace is reduced.~~**

17. (Original) The information handling system of Claim 16, wherein the first path is located at a distance from the ground plane that is substantially equal to the distance the second path is located from the voltage plane.

18. (Original) The information handling system of Claim 16, wherein the ground plane and the voltage plane are symmetrically oriented about the circuit board.

19. (Original) The information handling system of Claim 18, wherein the first path and the second path are symmetrically oriented about the circuit board.

20. (Original) The information handling system of Claim 19, wherein the first path and the ground plane are a mirror image of the second path and the voltage plane.